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10/596,448	06/14/2006	Katarzyna Leijten-Nowak	NL031466	6794

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,448	LEIJTEN-NOWAK, KATARZYNA	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

2. As for claims 1-10, applicant claims a method for creating an architecture of a reconfigurable logic core on an integrated circuit, comprising functional language that is descriptive of the created architecture, but does not comprise any clear method steps. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lien (US Patent 6,476,636).

4. As for the claims, Lien discloses the invention as claimed, including:

1. (original) A method for creating an architecture of a reconfigurable logic core on an integrated circuit [col. 1, line 59 – col. 2, line 3; col. 2, lines 14-32, and 48-67; col. 3, lines 1-10. NOTE that the examiner interprets the preceding portions of the Lien reference to disclose the method for creating the architecture of a reconfigurable logic core on an IC, including the use of a template or model, and including parameters for the description and realization of the architecture to its physical form because the programming of the device uses software programs which first represent the device as a template model that includes all of its parameters, connections, etc. in which the software representation ultimately programs the FPGA device to implement the design. Where the physical connections are present in the reference are directly modeled by the software in order to implement the device. Therefore, any physical connections of elements in the reference inherently include the template, model, and descriptions necessary to implement the device.]
the architecture comprising logic components, routing components and interface components [col. 5];
characterized in that the architecture is derived from a template [col. 1, line 59 – col. 2, line 3; col. 2, lines 14-32, and 48-67; col. 3, lines 1-10. NOTE A: the examiner interprets the preceding portions of the Lien reference to disclose the method for creating the architecture of a reconfigurable logic core on an IC, including the use of a template or model, and including parameters for the description and realization of the architecture to its physical form because the programming of the device uses software programs which first represent the device as a template model that includes all of its parameters, connections, etc. in which the software representation ultimately programs the FPGA device to implement the design. Where the physical connections are present in the reference are directly modeled by the software in order to implement the device. Therefore, any physical connections of elements in the reference inherently include the template, model, and descriptions necessary to implement the device];
the template being a model configured by a plurality of parameters [NOTE A];
wherein the model defines the logic components, the routing components and the interface components [col. 5; NOTE A];

the parameters having values and the values being in accordance with an application domain [NOTE A, specifically that the device is designed for a specific purpose];

2. (original) A method as claimed in claim 1, wherein the template comprises an array, the array comprising a plurality of logic tiles, and the number of logic tiles being a first parameter [NOTE A; col. 4, FPGA tiles];

3. (original) A method as claimed in claim 2, the aspect ratio of the array being a second parameter [NOTE A: col. 3, lines 13-29; col. 4; wherein the aspect ratio or spacing between elements has an at least inherent value, and also in col. 4, the various sizing and grouping of "tileable" FPGAs has an associate aspect ratio parameter];

4. (original) A method as claimed in claim 3, wherein the template further comprises:

at least one simple input/output tile, the simple input/output tile being coupled to a first logic tile [col. 3, lines 13-29, wherein the IGs are simple I/O tiles; fig. 5, elements IG 42];

at least one input/output tile with routing functionality, the input/output tile with routing functionality being coupled to a second logic tile [fig., 5, any of elements FG 40];

a corner routing tile, the corner routing tile being coupled to at least two input/output tiles [fig. 5, the corner elements FG 40];

5. (original) A method as claimed in claim 4, wherein at least one of the logic tiles comprises:

a logic block, the logic block comprising a plurality of logic block ports [fig. 5, elements FG 40, figs. 6-8 showing in more detail the elements FG40 of fig. 5, including logic block ports];

routing resources, the routing resources comprising:

a plurality of routing tracks [figs. 5-8; col. 3, lines 13-17; fig. 8-14 showing in detail the connections and routing between elements FG40; col. 5, describing the routing and structure of routing between elements FG40];

logic ports, the logic ports being arranged to couple the logic block ports to a neighboring logic tile [figs. 5-8; col. 3, lines 13-17; fig. 8-14 showing in detail the connections and routing between elements FG40; col. 5, describing the logic ports and structure of logic connections between elements FG40];

routing ports, the routing ports being arranged to couple the routing tracks to a neighboring logic tile [figs. 5-8; col. 3, lines 13-17; fig. 8-14 showing in detail the connections and routing between elements FG40; col. 5, describing the routing and structure of routing connections between elements FG40];
direct ports, the directs ports enabling a direct connection of the logic block with neighboring logic tiles [figs. 5-8; col. 3, lines 13-17; fig. 8-14 showing in detail the connections and routing between elements FG40; col. 5, describing the routing and structure of routing connections between elements FG40, especially the intra-tile global routing];
6. (original) A method as claimed in claim 5, wherein the logic block ports comprise first primary input ports, intermediate signals, control signals [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9] and the logic block further comprises:
a plurality of processing clusters, the number of processing cluster being a third parameter, wherein at least one of the processing clusters comprises a plurality of serially connected processing elements, the number of processing elements being a fourth parameter, and the processing cluster further comprising a plurality of first secondary input ports, a first carry input port and a first carry output port [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
a first multiplexer block, the first multiplexer block being arranged to be controlled by control signals issued by a first input selection block, the first multiplexer block being arranged to make a selection from first intermediate signals issued by the processing elements [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations,

Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
an output selection block, the output selection block being arranged to receive the selection of the first intermediate signals and to determine the number of output signals of the logic block, the output selection block further being arranged to generate the output signals and to send the output signals to output ports of the logic block [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
a flip-flop block, the flip-flop block being arranged to register the output signals [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
7. (original) A method as claimed in claim 6, wherein the first input selection block is arranged to couple the first primary input ports to second primary input ports, the second primary input ports being comprised in the processing elements, and to select input signals [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
the first input selection block further being arranged to accept output signals of the logic block as input signals such that a feedback loop is realized [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
8. (original) A method as claimed in claim 6, wherein at least one of the processing elements comprises:

a plurality of serially connected logic elements, the number of logic elements being a fifth parameter [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a plurality of second secondary input ports, the second secondary input ports being coupled to third secondary input ports comprised in the logic elements [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a second carry input port, the second carry input port being coupled to a third carry input port comprised in a first one of the serially connected logic elements [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a second carry output port, the second carry output port being coupled to a third carry output port comprised in a last one of the serially connected logic elements [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a plurality of first arithmetic output ports [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a first Boolean output port [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out

operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a second input selection block, the second input selection block being arranged to couple the second primary input ports to third primary input ports comprised in the logic elements, and to select input signals [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

a second multiplexer block, the second multiplexer block being arranged to be controlled by control signals issued by the second input selection block, the second multiplexer block being arranged to select signals originating from second Boolean output ports comprised in the logic elements, and the second multiplexer block further being arranged to produce an output signal for the first Boolean output port [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

wherein second arithmetic output ports comprised in the logic elements are coupled to the first arithmetic output ports [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

9. (original) A method as claimed in claim 8, wherein at least one of the logic elements comprises:

a plurality of third primary input ports, the number of third primary input ports being a sixth parameter [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];

the third carry input port or a further carry input port [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
the third carry output port or a further carry output port [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
one of the second Boolean output ports [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
- a plurality of the second arithmetic output ports, the number of second arithmetic output ports being a seventh parameter [figs 5-17; cols. 5-14, line 21 show and describe the logic block details, clustering, output selections, multiplexer operations, carry in carry out operations, Boolean operations, and flip-flop operations directed to the claimed coupling and operation of elements, especially in relation to claims 6-9];
10. (currently amended) A reconfigurable logic core having an architecture created by a method as claimed in claim 1 [see as cited in the rejection of claim 1].

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
September 5, 2008